Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Previously Presented) A method comprising:

receiving power control instructions via a first link in a first plurality of frames, the power control instructions being sent from a first station to a second station and used to adjust transmit power of the second station;

keeping a running history, up to a predetermined length, of the received power control instructions; and

generating power control bits for transmission via a second link in a second plurality of frames, the power control bits being sent from the second station at an effectual response rate based at least in part on the running history being kept for the power control instructions received via the first link, the effectual response rate being a function of the predetermined length and directly proportional to a batch processing rate of a batching process, wherein m "zero" value power control bits and n "one" value power control bits are generated for each batch formed with a subset of the second plurality of frames, with m and n being integers determined based on number of power control instructions with "0" value and number of power control instructions with "1" value in the running history.

2–4. (Canceled)

5. (Previously Presented) The method of claim 1, wherein m and n differ by 1 if each batch of the subset of the second plurality of frames contains an odd number of frames and if the number of power control instructions with "0" value is equal to the number of power control instructions with "1" value in the running history.

6. (Original) The method of claim 5, wherein m is greater than n by 1 for batches of odd ordinal positions in their order of formation, and n is greater than m by 1 for batches of even ordinal positions in their order of formation.

7. (Previously Presented) The method of claim 5, wherein m is greater than n by 1 for batches of even ordinal positions in their order of formation, and n is greater than m by 1 for batches of odd ordinal positions in their order of formation.

8. (Previously Presented) The method of claim 1, wherein said generating comprises alternating between generating "one" value power control bit and "zero" value power control bit for each batch formed with a subset of the second plurality of frames.

9. (Previously Presented) The method of claim 1, wherein if the running history includes two power control instructions of "11" for two frames received via the first link, each batch includes one extra "one" value power control bit if there are odd number of frames in each batch, and each batch includes two extra "one" value power control bits if there are even number of frames in each batch.

10. (Previously Presented) The method of claim 1, wherein each batch includes equal number of "zero" value power control bits and "one" value power control bits if the running history includes two power control instructions of "01" or "10" for two frames received via the first link and if there are even number of frames in each batch.

11. (Previously Presented) The method of claim 1, wherein if the running history includes two power control instructions of "00" for two frames received via the first link, each batch includes one extra "zero" value power control bit if there are odd number of frames in each batch, and each batch includes two extra "zero" value power control bits if there are even number of frames in each batch.

12. (Original) The method of claim 1, wherein said keeping and generating operations are being performed in a gateway of a wireless communication system.

13. (Original) The method of claim 1, wherein said keeping and generating operations are being performed in an emulated gateway and a gateway simulator of a wireless communication test system.

14. (Currently Amended) A gateway of a wireless communication system, comprising:

a transceiver to receive power control instructions in a first plurality of frames on a first link, the power control instructions being sent from a terminal to the gateway and used to adjust transmit power of the gateway; and

a processing subsystem coupled to the transceiver ~~subsystem~~

to receive the power control instructions outputted by the transceiver,

to keep a running history, up to a predetermined length, of the received power control instructions,

to generate power control bits for transmission via a second link in a second plurality of frames, to batch the second plurality of frames according to a batching process having a batch processing rate, to generate the power control bits based at least in part on the running history being kept for the received power control instructions, to generate m "zero" value power control bits and n "one" value power control bits for each batch formed with a subset of the second plurality of frames, with m and n being integers determined based on number of power control instructions with "0" value and number of power control instructions with "1" value in the running history, and

to send the power control bits at an effectual response rate, the effectual response rate being a function of the predetermined length and directly proportional to the batch processing rate.

15–17. (Canceled)

18. (Previously Presented) The gateway of claim 14, wherein the processing subsystem generates either one more "zero" value power control bit or one more "one" value power control bit for each batch of the subset of the second plurality of frames if each batch contains an odd number of frames and if the number of power control instructions with "0" value is equal to the number of power control instructions with "1" value in the running history.

19. (Original) The gateway of claim 18, wherein the processing subsystem is designed to generate one more "zero" value power control bit for batches of odd ordinal positions in their order of formation, and one more "one" value power control bit for batches of even ordinal positions in their order of formation.

20. (Previously Presented) The gateway of claim 18, wherein the processing subsystem is designed to generate one more "zero" value power control bit for batches of even ordinal positions in their order of formation, and one more "one" value power control bit for batches of odd ordinal positions in their order of formation.

21. (Previously Presented) The gateway of claim 14, wherein the processing subsystem alternates between generating "one" value power control bit and "zero" value power control bit for each batch formed with a subset of the second plurality of frames.

22. (Previously Presented) The gateway of claim 14, wherein if the running history includes two power control instructions of "11" for two frames received via the first link, the processing subsystem generates one extra "one" value power control bit in each batch if there are odd number of frames in each batch and generates two extra "one" value power control bits in each batch if there are even number of frames in each batch.

23. (Previously Presented) The gateway of claim 14, wherein the processing subsystem generates equal number of "zero" value power control bits and "one" value power control bits for each batch if the running history includes two power control instructions of "01" or "10" for two frames received via the first link and if there are even number of frames in each batch.

24. (Previously Presented) The gateway of claim 14, wherein if the running history includes two power control instructions of "00" for two frames received via the first link, the processing subsystem generates one extra "zero" value power control bit in each batch if there are odd number of frames in each batch and generates two extra "zero" value power control bits in each batch if there are even number of frames in each batch.

25. (Previously Presented) A wireless communication testing system, comprising:

a processor;

a gateway emulator to emulate a gateway including receipt of power control instructions in a first plurality frames on a first link, the power control instructions being used to adjust transmit power of the gateway; and

a gateway simulator coupled to the gateway emulator

to receive the power control instructions from the gateway emulator,

to maintain a running history, over a predetermined length, of the received power control instructions,

to generate power control bits for transmission via a second link in a second plurality of frames, to batch the second plurality of frames according to a batching process having a batch processing rate, to generate the power control bits based at least in part on the running history being kept for the received power control instructions, to generate m "zero" value power control bits and n "one" value power control bits for each batch formed with a subset of the second plurality of frames, with m and n being integers determined based on number of power control instructions with "0" value and number of power control instructions with "1" value in the running history, and

to send the power control bits at an effectual response rate, the effectual response rate being a function of the predetermined length and directly proportional to the batch processing rate.

26–28. (Canceled)

29. (Previously Presented) The wireless communication testing system of claim 25, wherein the gateway simulator generates either one more "zero" value power control bit or one more "one" value power control bit for each batch of the subset of the second plurality of frames if each batch contains an odd number of frames and if the number of power control instructions with "0" value is equal to the number of power control instructions with "1" value in the running history.

30. (Original) The wireless communication testing system of claim 29, wherein the gateway simulator is designed to generate one more "zero" value power control bit for batches of odd ordinal positions in their order of formation, and one more "one" value power control bit for batches of even ordinal positions in their order of formation.

31. (Previously presented) The wireless communication testing system of claim 29, wherein the gateway simulator is designed to generate one more "zero" value power control bit for batches of even ordinal positions in their order of formation, and one more "one" value power control bit for batches of odd ordinal positions in their order of formation.

32. (Previously Presented) The wireless communication testing system of claim 25, wherein the gateway simulator alternates between generating "one" value power control bit and "zero" value power control bit for each batch formed with a subset of the second plurality of frames.

33. (Previously Presented) The wireless communication testing system of claim 25, wherein if the running history includes two power control instructions of "11" for two frames received via the first link, the gateway simulator generates one extra "one" value power control bit in each batch if there are odd number of frames in each batch and generates two extra "one" value power control bits in each batch if there are even number of frames in each batch.

34. (Previously Presented) The wireless communication testing system of claim 25, wherein the gateway simulator generates equal number of "zero" value power control bits and "one" value power control bits for each batch if the running history includes two power control instructions of "01" or "10" for two frames received via the first link and if there are even number of frames in each batch.

35. (Previously Presented) The wireless communication testing system of claim 25, wherein if the running history includes two power control instructions of "00" for two frames received via the first link, the gateway simulator generates one extra "zero" value power control bit in each batch if there are odd number of frames in each batch and generates two extra "zero" value power control bits in each batch if there are even number of frames in each batch.

36. (Currently Amended) ~~Apparatus~~ A computing apparatus comprising:

means for receiving, with the computing apparatus, power control instructions via a first link in a first plurality of frames, the power control instructions being sent from a first station to ~~a second station~~ the computing apparatus and used to adjust transmit power of the ~~second station~~ computing apparatus;

means for keeping a running history, up to a predetermined length, of the received power control instructions; and

means for generating, with the computing apparatus, power control bits for transmission via a second link in a second plurality of frames, the power control bits being sent at an effectual response rate based at least in part on the running history being kept for the power control instructions received via the first link, the effectual response rate being a function of the predetermined length and directly proportional to a batch processing rate of a batching process, wherein m "zero" value power control bits and n "one" value power control bits are generated for each batch formed with a subset of the second plurality of frames, with m and n being integers determined based on number of power control instructions with "0" value and number of power control instructions with "1" value in the running history.

37. (Currently Amended) A non-transitory storage device storing thereon machine executable instructions that when executed implement a method comprising:

receiving power control instructions via a first link in a first plurality of frames, the power control instructions being sent from a first station to a second station and used to adjust transmit power of the second station;

keeping a running history, up to a predetermined length, of the received power control instructions; and

generating power control bits for transmission via a second link in a second plurality of frames, the power control bits being sent at an effectual response rate based at least in part on the running history being kept for the power control instructions received via the first link, the effectual response rate being a function of the predetermined length and directly proportional to a batch processing rate of a batching process, wherein m "zero" value power control bits and n "one" value power control bits are generated for each batch formed with a subset of the second plurality of frames, with m and n being integers determined based on number of power control

instructions with "0" value and number of power control instructions with "1" value in the running history.

38. (Currently Amended) A non-transitory storage device storing thereon machine executable instructions that when executed implement a method comprising:

emulating a gateway including receipt of power control instructions in a first plurality frames on a first link, the power control instructions being used to adjust transmit power of the gateway;

emulating a gateway simulator to receive the power control instructions,

to keep a running history, up to a predetermined length, of the received power control instructions,

to generate power control bits for transmission via a second link in a second plurality of frames, to batch the second plurality of frames according to a batching process having a batch processing rate, to generate the power control bits based at least in part on the running history being kept for the power control instructions received via the first link, to generate m "zero" value power control bits and n "one" value power control bits for each batch formed with a subset of the second plurality of frames, with m and n being integers determined based on number of power control instructions with "0" value and number of power control instructions with "1" value in the running history, and

to send the power control ~~bit~~ bits [[-]] at an effectual response rate, the effectual response rate being a function of the predetermined length and directly proportional to the batch processing rate.